Appl. No. 10/735,549
Amdt. dated June 29, 2006
Reply to final Office action of April 5, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.   (Currently amended) A system, comprising:

a central processing unit (CPU);

a graphical user interface (GUI) coupled to the CPU; and

a memory coupled to the CPU, wherein the memory stores a bump map application and a data extraction application executed by the CPU, wherein the bump map application displays a plurality of editable textual character groups representative of a plurality of bumps, the textual character groups are arranged on the GUI according to a relative coordinate position of the bumps with respect to an origin;

wherein the memory also stores a track definition application executed by the CPU, the track definition application displaying[[,]] on the GUI, individual track definitions and a macro that defines a plurality of editable numeric parameters corresponding to tracks of an integrated circuit metal layer; and[[,]]

wherein the data extraction application automatically extracts data from the bump map application and the track definition application for use by a router application.

2.   (Original) The system of claim 1 further comprising an input device coupled to the CPU, wherein the input device is used with the bump map application such that a user is able to change a position of each textual character group displayed on the graphical user interface.

3.   (Original) The system of claim 2 wherein the input device permits the user to edit textual characters of the textual character groups.

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4.   (Original) The system of claim 1 wherein the bump map application further displays a plurality of cells, wherein each cell is adapted to contain a textual character group.

5.   (Original) The system of claim 4 wherein each cell comprises information regarding a two-dimensional space.

6.   (Original) The system of claim 4 wherein each cell is shaded in one of a plurality of colors, wherein each color signifies information to a user.

7.   (Previously presented) The system of claim 1 wherein the track definition application displays on the GUI one or more sets of intersecting columns and rows containing editable information that describes tracks of an integrated circuit.

8.   (Original) The system of claim 7 wherein the bump map application and the track definition application are a single application that uses a single source file.

9.   (Previously presented) The system of claim 7 wherein the data extraction application extracts track-related data from the track definition application and organizes the track-related data for use by the router application.

10.   (Original) The system of claim 7 wherein at least one of the sets of intersecting columns and rows displays information selected from the group consisting of:

      a name associated with a set of intersecting rows and columns;

      a metal layer associated with a set;

      a label associated with a track;

      a width of the track;

      a space requirement on a left side of the track;

      a space requirement on a right side of the track;

an offset of the track from a predetermined origin;

a pitch between tracks; and

comments related to the track.

11.   (Previously presented) The system of claim 7 wherein at least one of the sets of intersecting columns and rows comprises a macro definition, wherein a plurality of track parameters contained in the macro definition are automatically entered using a predetermined macro label.

12.   (Original) The system of claim 11 wherein at least one of the sets of intersecting columns and rows contains a name associated with the macro definition and coordinates defining a two-dimensional region, wherein track parameters associated with the macro are used by a router application to lay out tracks in the two-dimensional region.

13.   (Original) The system of claim 1 wherein the origin is associated with an integrated circuit layout.

14.   (Currently amended) A method of extracting information for bumps and tracks of an integrated circuit, comprising;

creating a data structure;

extracting bump locations into the data structure from relative physical positions of bump labels in a table, wherein each bump label is associated with a bump;

determining if a macro defining a plurality of tracks exists;

if a macro defining a plurality of tracks exists, extracting track parameters into the data structure based on the macro; and

if a macro defining a plurality of tracks does not exist, extracting track parameters into the data structure based on individual track definitions.

15.   (Original) The method of claim 14 further comprising extracting at least one type of data contained in the table selected from the group consisting of:

      spacing between bumps;

      size of bumps; and

      bump labels.

16.   (Original) The method of claim 14 further comprising extracting coordinate positions of input/output circuitry of an integrating circuit into the data structure.

17.   (Original) The method of claim 16 further comprising:

      writing out the bump data and the coordinate positions of the input/output circuitry to a router application; and

      displaying straight-line connections between locations of bumps and locations of input/output circuitry associated with each bump.

18.   (Canceled).

19.   (Previously presented) The method of claim 14 further comprising:

      writing out the bump data, the coordinate positions of the input/output circuitry, and the track parameters to a router application; and

      displaying bumps, input/output circuitry locations, and tracks to a user according to the bump data, the coordinate positions of the input/output circuitry, and the track parameters.

20.   (Original) The method of claim 19 further comprising editing at least one type of data selected from the group consisting of the bump data and the track parameters in response to said displaying by accessing a single source file.

21.-25. (Canceled).

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26.   (Previously presented) A system, comprising:

a CPU;

a graphic user interface coupled to the CPU; and

a memory coupled to the CPU, wherein the memory comprises computer
readable instructions that when executed by the CPU provide:

means for displaying bump positions on the graphic user
interface using textual bump labels, wherein a
location of a displayed bump label corresponds to a
position of a bump relative to a predetermined origin
of an integrated circuit;

means for extracting the bump positions by interpreting
locations of the bump labels displayed on the
graphical user interface for use by a router
application; and

means for editing the textual bump labels by displaying
straight-line connections between bumps and
input/output circuitry prior to displaying tracks
between the bumps and input/out circuitry.

27.   (Original) The system of claim 26 wherein the computer readable
instructions when executed by the CPU further provide means for condensing
editable metal layer information viewable to a user.

28.   (Original) The system of claim 27 wherein the computer readable
instructions when executed by the CPU further provide means for extracting the
condensed editable metal layer information for use by a router application.